UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,059	01/15/2004	Zhongze Wang	400.147US02	5110

27073 7590 12/22/2005

LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
PHAM, THANH V	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,059	WANG ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7,14,15,26,27 and 36* is/are allowed.

6)☒ Claim(s) *1,5,6,8,12,13,16,19-25,28,31-35,37,41-49,51-53,56 and 57* is/are rejected.

7)☒ Claim(s) *2-4,9-11,17,18,29,30,38-40,50,54 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

instant [0001]'s line 3, "(allowed)" should be –now US 6,716,687—to indicate the current status of application 10/073,723;

instant [0020] discloses "sidewall oxidation either before or after deposition of layer 20" and "the sidewall oxidation may be performed prior to formation of layer 16"; these two steps (the underlined parts) cannot be performed as stated. It is suggested that "or after " is deleted and "16" is changed to –20--;

In [0030]'s line 7, "26" should be –46--;

Elements 54 in fig. 1J are not defined anywhere in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5-6 and 47-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Subramanian et al. US 5,481,126.

The Subramanian et al. reference discloses a FET (fig. 3L) comprising: a channel region 25 in a bulk semiconductor substrate 10; a first and second S/D region on sides

of the channel region 25, col. 5, lines 27-44; an extension of epitaxial silicon 32 formed on the bulk semiconductor substrate so as to extend away from each side of the channel region 25; a field isolation region 30 laterally adjoining the first and second S/D region and extending beneath at least of the first and second S/D region. The bulk semiconductor substrate comprises monocrystalline silicon having a first conductivity type (col. 3, line 60), the conductivity type of the epitaxial silicon is the second conductivity type (col. 5, lines 27-44).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8, 12-13, 37 and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al. as applied to claims 1, 5-6 and 47-49 above, and further in view of Jacob Millman, Microelectronics: Digital and Analog Circuits and Systems, McGraw-Hill, 1979, pp. 289, 295.

The Subramanian et al. reference discloses a FET structure as in the above but does not disclose that FET is comprised in a memory device or an electronic system with a processor and word/bit lines wherein the FET is an access transistor. However, the use of FET as a component of a system and/or memory device is disclosed in the art as in Jacob Millman's figs 9-18 and 9-22 in pages 289 and 295 respectively. It would

have been obvious to one of ordinary skill in the art at the time of the invention to provide the system and memory device of the Millman reference with the FET of Subramanian et al. because the semiconductor electronic device of Subramanian et al. would provide the system and memory device of Millman with typical FET useful in memory device.

6. Claims 16, 19-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al. as applied to claims 1, 5-6 and 47-49 above, and further in view of Wieczorek et al. US 6,274,894 B1.

The Subramanian et al. reference discloses a FET structure as in the above but does not disclose that FET comprising SiGe in the S/D regions. The Wieczorek et al. teaches (figs. 9, 12, 15 and associated passages) extensions of SiGe are grown in trenches 52 on two sides of the channel to form S/D regions. It would have been obvious to one of ordinary skill in the art at the time of the invention to employ SiGe for the S/D 32 of Subramanian et al. because it is well settle that "the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945)", MPEP 2144.07. Further, choice of ratio of Si and Ge in the SiGe material to achieve particular device properties would have been a matter of routine optimization because at% of either Si or Ge in SiGe are known to affect the device properties and would depend on the desired device density on the finished wafer and the desired

device characteristics. One of ordinary skill in the art would employ the claimed 20-50 at% of Ge through routine experimentation to achieve desired device characteristics.

7. Claims 28,31-35, 37, 41-46, 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Subramanian et al. as applied to claims 1, 5-6 and 47-49 and/or the combination of Subramanian et al. with Wieczorek et al. as applied to claims 16, 19-25 above, and further in view of Jacob Millman, Microelectronics: Digital and Analog Circuits and Systems, McGraw-Hill, 1979, pp. 289, 295.

The Subramanian et al. and/or the combination of Subramanian et al. with Wieczorek et al. reference discloses a FET structure as in the above but does not disclose that FET is comprised in a memory device or an electronic system with a processor and word/bit lines wherein the FET is an access transistor. However, the use of FET as a component of a system and/or memory device is disclosed in the art as in Jacob Millman's figs 9-18 and 9-22 in pages 289 and 295 respectively. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the system and memory device of the Millman reference with the device of the combination of Subramanian et al. with Wieczorek et al. because the semiconductor electronic device of the combination would provide the system and memory device of Millman with typical FET useful in memory device.

Allowable Subject Matter

8. Claims 7, 14-15, 26-27 and 36 are allowed.

9. Claims 2-4, 9-11, 17-18, 29-30, 38-40, 50 and 54-55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the cited prior art, individually or in combination, does not disclose or suggest all of the claimed elements in the present application. Although instant' [025] discloses a would-be-phenomenon in the step of growing epitaxial silicon on the exposed surfaces of the bulk/monocrystalline

> "Others have observed that silicon mobility is enhanced by the presence of halides in the reaction gases. Other factors recognized to enhance the selective mature of the silicon deposition include reduced reaction pressure, increased reaction temperature and decreased mol fraction of silicon in the reaction gases. Some polysilicon growth may occur concurrently with the epitaxial growth due to reactions occurring on non-monocrystalline surface, e.g., exposed surfaces of the dielectric material".

Instant specification does not provide any motivation to make the combination for the above references such that the epitaxial silicon interposed between the channel region and the S/D regions having partial polysilicon and the epitaxial silicon being doped with germanium.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVP

12/20/2005

George Fourson
Primary Examiner